REMARKS

This responds to the Office Action mailed on February 24, 2005, and the references cited therewith.

Claims 15, 20, 24, 25, 33, and 34 are amended, claims 26-28 are canceled, and no claims are added; as a result, claims 1-25 and 29-33 are now pending in this application.

Claims 28 and 29

As the Examiner noted (page 2, item 2, of the Office Action), in the previous response filed by Applicant on 11/24/2004, the versions presented of claims 28 and 29 presented were not correct. Applicant has cancelled claim 28, and accordingly this notice is moot with respect to that claim. With respect to claim 29, Applicant has corrected this inadvertent error by including the correct version of claim 29, as it has been amended to date, in this response. Applicant apologizes for any inconvenience that this error may have caused.

Claim Interpretations

On pages 2-3 and elsewhere within the Office Action, the Examiner sets forth a number of interpretations of claim terms. Applicant does not necessarily agree with the interpretations, and reserves the right to challenge those interpretations, either directly or indirectly, in this or a future correspondence or legal action. Applicant's silence with respect to any particular claim interpretation should not be construed as Applicant's agreement or acceptance of the claim interpretation.

§102 Rejection of the Claims

Claims 1-8, 12-30, and 33 were rejected under 35 U.S.C. § 102(b) for anticipation by IEEE 1364-1995 – IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language (herein "IEEE 1364"). Applicant has amended claims 15, 20, 24, 25, and 33, has cancelled claims 26-28, and respectfully traverses the rejection.

In Applicant's previous response, filed 11/24/2004, Applicant traversed this rejection on the grounds that IEEE 1364 does not include Applicant's claim elements arranged as set forth in

the claims. Applicant further requested that the Examiner provide citations in IEEE 1364 showing Applicant's claim elements arranged as they are set forth in the claims.

In the Office Action section entitled "Response to Amendment filed 11/24/2004," specifically in section 76, page 36, the Examiner has acknowledged this request, and has indicated that the Examiner provided more detail in the rejection. In particular, the Examiner provided the following citation (Office Action, page 5):

> "Section 9, pp. 104 teaches that 'A force statement to a register shall override a procedural assignment or procedural continuous assignment that takes place on the register until a release procedural statement is executed on the register. After the release procedural statement is executed, the register shall not immediately change value (as it would a net that is forced). The value specified in the force statement shall be maintained in the register until the next procedural assignment takes place, except in the case where a procedural continuous assignment is active on the register.'"
> (*See* IEEE 1364, Section 9, pp. 104-106)

Applicant appreciates the Examiner's consideration of the request for citations in IEEE 1364. However, Applicant does not believe that the above citation discloses Applicant's claim elements arranged as set forth in the claims.

The above citation indicates the following sequence of steps:

- a procedural assignment or a procedural continuous assignment takes place on a register,
- a force statement is executed on the register, which overrides the procedural assignment,
- a release procedural statement is executed on the register,
- the register does not change value until the next procedural assignment takes place, except where a procedural continuous assignment is active on the register.

In contrast, Applicant's claim 1 discloses the following (limitations of claims 8, 15, 20, 24, 25, 33, and the claims that depend from them are similar):

". . . executing a first circuit module that simulates a circuit having a node . . .;

simultaneously executing at least one behavior module, . . . which performs the acts of

forcing an initial forced logic state on the node;

after forcing, releasing the node from the initial forced logic state . . .;

monitoring the node after the node has been released; and

providing an indication, in response to the monitoring, when the node is in a preselected condition." (claim 1)

A first distinction is that the citation within IEEE 1364, given above, applies to "registers" and not to "nodes." Accordingly, Applicant does not believe that the IEEE 1364 citation is applicable to the sequence claimed in claim 1.

Further, Applicant contends that IEEE 1364 does not disclose the algorithmic relationship claimed in claim 1 of "executing a first circuit module" and "simultaneously executing at least one behavior module."

Applicant believes that the governing rule is that: "Anticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

IEEE 1364 describes various definitions relating to Verilog HDL. This is analogous to a textbook that lists the commands associated with a software language (e.g., C++), and which describes the syntax for those commands.

However, IEEE 1364 does not describe the arrangements of processes, apparatus, or means elements claimed in the present application. In other words, IEEE 1364 does not describe the underlying algorithm of applicants claims. IEEE 1364 merely describes a collection of disjointed definitions.

Applicant believes that the arguments presented above also apply to claims 2-8, 12-25, 29, 30, and 33, which were rejected together with claim 1 under 35 U.S.C. § 102(b). More

specifically, IEEE 1364 does not disclose the portions of the algorithms in claims 2-8, 12-25, 29, 30, and 33.

For these reasons, Applicant does not consider IEEE 1364 as disclosing each and every element of the claimed invention, arranged as they are in the claims. Because claims 26-28 have been cancelled, the rejection of these claims under 35 U.S.C. § 102(b) is moot. Applicant respectfully requests that the Examiner reconsider the rejection under 35 U.S.C. § 102(b), in light of Applicant's clarifications above, and allow claims 1-8, 12-25, 29, 30, and 33.

§103 Rejections of the Claims

Claims 1, 8, 15, 20, 25, 28, and 29:

Claims 1, 8, 15, 20, 25, 28, and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over QuickNote #61 in view of Official Notice. Applicant has amended claims 15, 20, and 25, has cancelled claim 28, and respectfully traverses the rejection.

QuickNote #61 discloses a method for initializing a flip-flop (or flip flops) during a design simulation. (See p. 1, "Reasons for Initializing Flip Flops"). QuickNote #61 states that "The Verilog simulator . . . allows the ability to force internal signals in the design to desired values for desired periods of time. If you want to set an internal node called DRAM_CONTROLX to a value of '1', for example, you can create a small Verilog initial block in the Verilog test-fixture (.TF) file used to simulate the design." (See p. 1, "Using the simulator to set initial values for flip-flops").

The Office Action states, on pages 19-20, that QuickNote #61 teaches the limitations of claim 1 of "executing a first circuit module. . .", "simultaneously executing at least one behavior module . . .", "forcing an initial forced logic state on the node . . ." and "after forcing, releasing the node . . . if a predetermined condition is met." Applicant respectfully disagrees.

Instead of teaching the limitations of Applicant's claims, listed above, QuickNote #61 teaches: "initializing a flip-flop . . . during simulation" (p. 1, "Reasons . . ."), and creating a Verilog initial block, which forces a node to a specific value (e.g., "force m.DRAM_CONTROLX = 1'b1") for a number of time units (e.g., "#100"), and then releases the node (e.g., "release m.DRAM_CONTROLX"). (See pp. 1-2, "Using the simulator . . .").

Applicant believes that this disclosure is different from that which is claimed in Applicant's claims.

Further, the Office Action took Official Notice that it would have been obvious to one or ordinary skill in the art at the time the invention was made to perform the steps of "monitoring the released node . . ." and "providing an indication, in response to monitoring, when the node is in a pre-selected condition." Applicant respectfully traverses this Official Notice and requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d) (2).

Further, the Office Action, on page 20, states: "QuickNote #61 teaches (p. 1, 1st para.) that 'Another reason for initializing flip-flops is that a free-running toggle flip-flop or divider circuit may never leave the unknown state unless it is manually initialized.' There is always a possibility that once a node is released, it 'relapses' into an unknown state, in which case some sort of error message would be beneficial."

Applicant begs the Examiner's patience, but fails to see how this applies to the elements of "monitoring the released node . . ." and "providing an indication, in response to monitoring, when the node is in a pre-selected condition." The reference in QuickNote #61 pertains to reasons for initializing flip-flops in an unknown state. It does not pertain to: "forcing an initial forced logic state on the node; after forcing, releasing the node from the initial forced logic state . . .; monitoring the node after the node has been released; and providing an indication, in response to the monitoring, when the node is in a preselected condition." (claim 1). Applicant respectfully requests that, if this argument is repeated, the Examiner indicate how the teachings of QuickNote #61 apply to these claim elements.

Based on the reasoning presented above, Applicant believes that the rejection of claims 1, 8, 15, 20, 25, and 29 under 35 U.S.C. § 103(a) have been overcome. Because claim 28 has been cancelled, the rejection of this claim under 35 U.S.C. § 103(a) is moot. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection, and allow claims 1, 8, 15, 20, 25, and 29.

Claims 9-11, 34, and 35:

Claims 9-11, 34, and 35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over IEEE 1364 in view of IEEE 1164 and further in view of Smith and further in view of Berman. Applicant has amended claim 34, and respectfully traverses the rejection.

Claims 9-11 are dependent from claim 8, which was rejected under 35 U.S.C. § 102(b) for anticipation by IEEE 1364. As Applicant has pointed out in detail in response to the rejection of claim 8, IEEE 1364 does not disclose the features of claim 8. Nor, as the Office Action indicates, does it disclose the features of claims 9-11. If this rejection is repeated, Applicant reserves the right to provide additional arguments with respect to the allowability of claims 9-11, and particularly arguments that address the additional references cited against claims 9-11 (i.e., IEEE 1164, Smith, and Berman).

With respect to claims 34 (from which claim 35 depends), and for reasons analogous to those set forth in the response to the rejection of the claims under 35 U.S.C. § 102(b), nowhere do IEEE 1364, IEEE 1164, Smith, Berman, or their combination disclose, suggest or motivate:

". . . executing phase one by a behavior module, including

forcing an initial logic zero, logic one or high-impedance on a node of a circuit module linked with the behavior module. . .,

releasing the node, . . . wherein releasing occurs after forcing,

testing to see if the node has a valid logic value, wherein testing occurs after releasing,

if the node has the valid logic value, continuing to phase two, and

if the node does not have the valid logic value, continuing in phase one; and

simultaneously executing phase two by the behavior module, including

monitoring the node value,

testing the node value for a valid condition,

indicating an error if an unacceptable condition appears on the node, in response to monitoring and testing, and

continuing in phase two until simulation completion."

(claim 34)

Further, the Office Action provides no evidence of record of a suggestion or motivation to combine IEEE 1364, IEEE 1164, Smith, and/or Berman. The Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). Applicant respectfully submits that the Office Action has not provided objective evidence for a suggestion or motivation to combine the references.

Based on the reasoning presented above, Applicant believes that the rejection of claims 9-11, 34, and 35 under 35 U.S.C. § 103(a) have been overcome. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection, and allow these claims.

Claims 31 and 32:

Claims 31 and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over IEEE 1364 in view of *In re Kuhle*. Applicant respectfully traverses the rejection.

For reasons analogous to those set forth in the response to the rejection of the claims under 35 U.S.C. § 102(b), nowhere do IEEE 1364, *In re Kuhle*, or their combination disclose, suggest or motivate:

". . . a circuit HDL module, which when executed simulates a circuit having a first simulated node. . .;

a first HDL module, linked to the circuit HDL module, the first HDL module including

a first input submodule inputting a first initial node condition,

a first conveyance submodule conveying the first initial node condition to the first simulated node,

a first monitor submodule monitoring the first simulated node for a first node condition, wherein monitoring occurs after conveying, and

a first output submodule outputting, in response to monitoring, a first indication when the first node condition is in an undesirable state;

a second HDL module, linked to the circuit HDL module, the second HDL module including

a second input submodule inputting a second initial node condition,

a second conveyance submodule conveying the second initial node condition to a second simulated node,

a release submodule releasing the second simulated node on a predetermined condition, wherein releasing the second simulated node enables a simulation program to change a logic level of the second simulated node,

a second monitor submodule monitoring the second simulated node for a second node condition, wherein monitoring occurs after releasing, and

a second output submodule outputting, in response to monitoring, a second indication when the second node condition is in an undesirable state; and

wherein the first conveyance submodule additionally conveys the first initial node condition to the second input submodule."

(claim 31)

OR

". . . a circuit HDL module. . .;

a first HDL module , linked to the circuit HDL module, the first HDL module including

a first input means for inputting a first initial node condition,

a first conveyance means for conveying the first initial node condition to the first simulated node, and

a first node condition output means for outputting a first indication when a first node condition is in an undesirable state, wherein outputting occurs after conveying;

a second HDL module, linked to the circuit HDL module, the second HDL module including

a second input means for inputting a second initial node condition, and

a second conveyance means for conveying the second initial node condition to a second simulated node; and

a third HDL module, linked to the circuit HDL module, the third HDL module including

a release condition means for releasing the second simulated node on a release condition, wherein releasing the second simulated node occurs after conveying and enables a simulation program to change a logic level of the second simulated node,

wherein the first node condition output means outputs the first node condition to the second input means if the release condition is valid."

(claim 32)

Further, the Office Action provides no evidence of record of a suggestion or motivation to combine IEEE 1364 and *In re Kuhle*. The Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). Applicant respectfully submits that the Office Action has not provided objective evidence for a suggestion or motivation to combine the references.

Based on the reasoning presented above, Applicant believes that the rejection of claims 31 and 32 under 35 U.S.C. § 103(a) have been overcome. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection, and allow these claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Sherry Schumm, at (480) 538-1735 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

BOHR-WINN SHIH ET AL.

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Date June 24, 2005

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24 day of June, 2005.

Tina Kohut
Name

Signature